Code: 9A05406

1

B.Tech III Year I Semester (R09) Regular & Supplementary Examinations December/January 2013/14

COMPUTER ORGANIZATION

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Distinguish between high level and low level languages. What are the requirements for a good programming language?

(b) Explain in brief about Amdahl's law.

2 (a) Design a 4 bit combinational circuit decrementer using four full-adder circuits.

(b) The following transfer statements specify a memory. Explain the memory operation in each case:

(i) $R_2 \leftarrow M[AR]$

(ii) $M[AR] \leftarrow R_3$

(iii) $R_5 \leftarrow M[R_5]$

3 (a) Discuss in brief about the functioning of micro-programmed control unit.

(b) List the advantages and disadvantages of micro-programmed control unit.

4 (a) Explain the hardware for signed 2's complement addition and subtraction.

(b) Perform the following in 2's complement form:

(i) $(+28)_{10} + (+15)_{10}$

(ii) $(+28)_{10} + (-15)_{10}$

(iii) $(-28)_{10} + (+15)_{10}$

(iv) $(-28)_{10} + (-15)_{10}$

5 (a) Explain memory hierarchy in detail.

(b) Explain the concept of content addressable memory. How the time for read/write operation is minimized in associative memory?

6 (a) What are the two formats of data transfer?

(b) Draw the basic structure of serial data format.

7 (a) Explain the advantages and disadvantages of RISC and CISC architecture.

(b) List the applications of array processors.

8 (a) Explain the characteristics of multiprocessors.

(b) Give a short note on cache coherence.

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1 (a) Explain pipelining and superscalar operation and how it will affect the performance of computer.

(b) Discuss in brief about multiprocessors and multicomputers.

2 (a) Explain three address, two address, one address and zero address instructions with examples.

(b) Write a program to evaluate the arithmetic statement Y=(A+B)*(C+D) using three address, two address and zero address instructions.

3 (a) What is nanomemory? Explain nanoinstruction sequencing organization with flow chart.

(b) What are the advantages and disadvantages of nanoprogramming?

4 (a) Explain the floating point addition and subtraction with flow chart.

(b) Show how the following floating point operations are performed (where significants are truncated to 4 decimal digits)

(i) $(0.2255 \times 10^{2}) \times (0.1234 \times 10^{1})$

(ii) $(0.8833 \times 10^{3}) \div (0.5555 \times 10^{5})$

5 (a) Explain the concept of virtual address and physical address.

(b) Explain RAID levels with neat sketches.

6 (a) Explain the methods of priority resolution for interrupts.

(b) Explain the data transfer using handshake procedure between CPU and I/O devices.

7 (a) What is pipeline? Explain space-time diagram for pipeline.

(b) Explain pipeline for floating point addition and subtraction.

8 What is the Flynn's classification of the computer system? Explain in detail.

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1 (a) Explain IEEE 754 representation of floating point numbers.

(b) Represent the number $(+46.5)_{10}$ as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits.

(c) Perform the following arithmetic operations using 10's complement representation.
(i) (-638) + (+785). (ii) (-638) – (+185).

2 (a) Draw and explain about the instruction cycle state diagram.

(b) Describe various arithmetic and logical instruction set operations.

3 (a) What is the necessity of branching? Explain the control sequence required for branch instruction.

(b) Give the horizontal and vertical micro instructions format and compare them.

4 (a) Explain Booth's algorithm with flow chart.

(b) Explain how Booth's algorithm is suitable for signed number multiplication in comparison of conventional shift and add method.

5 (a) What is a virtual memory? Explain its features.

(b) Explain the concept of ROM.

6 (a) Explain DMA. Describe about functions of DMA.

(b) Explain handshaking in asynchronous data transfer.

7 Explain the following in detail:

(a) Data dependencies.

(b) Hardware interlocks.

(c) Operand forwarding.

8 (a) Explain the functioning of omega switching network with a neat sketch.

(b) In 8 x 8 omega switching network how many stages are there and in each stage how many switches are there.

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Time: 3 hours Max Marks: 70

Answer any FIVE questions

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1 (a) Explain with the help of diagram the connections between processor and main memory.

(b) A computer uses a memory unit with 4K words of 8 bits each. The computer wants to read data from the memory location 2000H. The data stored in memory location 2000H is 32H.
(i) What is the size of address bus?
(ii) What is the size of data bus?
(iii) What are the contents of memory address register?
(iv) What are the contents of memory data register?
(v) What are the contents of program counter?
(vi) What are the contents of Instruction register?

2 (a) Explain the interrupt cycle with the help of flowchart.

(b) Draw and explain the input-output configuration of a basic computer.

3 (a) Explain in detail the block diagram for hardwired control unit.

(b) What are the design methods of hardwired control unit? Explain any two methods.

4 (a) Explain the operation of BCD adder with the help of diagram.

(b) Explain mantissa overflow, mantissa underflow, exponent overflow and exponent underflow.

5 To construct a memory unit with capacity of 4096 bytes, only 128 x 8 RAM chips are available, how many of them are used to get the memory capacity. If so how many address lines are needed to access the memory and how many lines are needed to access each chip.

6 Explain the following in detail:
(a) IEEE 1394.
(b) I/O Interface.
(c) IOP serial communication.

7 (a) Explain the process of arithmetic pipelining with an example.

(b) Explain the terms data dependencies, hardware interlock and operand forwarding techniques.

8 (a) Explain multiport memory organization with a neat sketch.

(b) Explain system bus structure for multiprocessors with a neat sketch.

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