**Code: 13A05401** **R13**

B.Tech III Year I Semester (R13) Regular Examinations December 2015

**COMPUTER ORGANIZATION & ARCHITECTURE**

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is the use of program counter?
(b) Explain software and hardware interrupts.
(c) Define effective address.
(d) Write any two main features of Booth's algorithm.
(e) How does high-impedance state behaves in bus system?
(f) Define pipeline register.
(g) Explain the need of bootstrap loader.
(h) What is an I/O interface?
(i) Describe resource conflicts in instruction pipeline.
(j) Define tightly coupled multiprocessor.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 (a) How the data can be read from memory? Explain with timing diagrams for memory read and memory write operations.
(b) Explain briefly the three categories of computer programming languages.

**OR**

3 (a) Explain briefly about the two commonly used organizations for multi-byte data organization.
(b) What are the different addressing modes used in assembly language instructions?

**UNIT – II**

4 Explain the way that the interrupts are handled by the computer by means of a flow chart.

**OR**

5 (a) Explain LDA and STA memory-reference instructions with suitable examples.
(b) Describe briefly about the register organization for floating point operations.

**UNIT – III**

6 (a) Define register transfer language. Explain the instructions with suitable examples.
(b) With a neat diagram explain 4-bit binary incrementer.

**OR**

7 (a) Explain how to construct a common bus for four registers of n bits each using three state buffers.
(b) What are the address sequencing capabilities required in the control memory? Explain.

**UNIT – IV**

8 (a) Draw and explain the block diagram of typical Ram chip.
(b) What are the major differences between that exists between the central computer and peripherals.

**OR**

9 (a) Explain briefly about the direct mapping cache organization.
(b) Discuss in detail about the Daisy-Chain priority interrupt.

**UNIT – V**

10 (a) What are the major difficulties that cause the instruction pipeline to deviate from its normal operations? Explain.
(b) Explain briefly about the characteristics of multiprocessors.

**OR**

11 (a) Describe briefly about the Flynn's classification of parallel processing systems.
(b) Explain in detail about the Hypercube interconnection structure.

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