I/O SUBSYSTEM ORGANIZATION AND INTERFACING

- CPU treats memory as homogeneous.
- I/O devices are very different. A PC Keyboard & hard disk perform different function, yet both are part of the I/O subsystem.
- Each I/O device is connected to system buses. Each I/O device includes I/O interface circuitry, actually this circuitry interacts with the buses & also interacts with the actual I/O device to transfer data.

AN INPUT DEVICE: A) WITH ITS INTERFACE B) THE ENABLE LOGIC FOR THE TRI-STATE BUFFERS

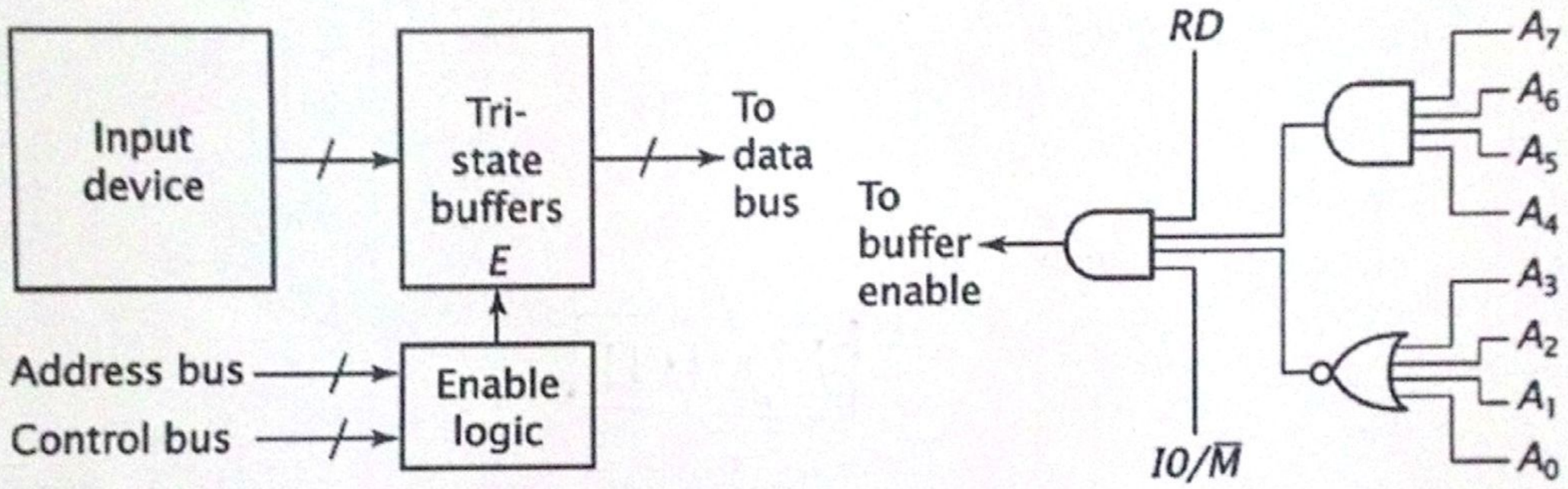


Fig 1.10

- The above fig fig 1.10 shows the generic interface circuitry for an input device such as a keyboard.
- The data from i/p device goes to tristate buffer. when the values on the address bus & control bus are correct the buffers are enabled and data pases onto data bus
- when this values are not correct logic block does not enable the buffers; they are tristated and donot place data onto the bus.
- The key to this design is enable logic. Each I/O device has unique address. The enable logic must not enable the buffers unless it receives the correct address from the address bus. It must also get correct control signals from control bus. For an i/p device RD signal must be asserted as well as IO/$\overline{M}$ signal.
- Fig 1.10a shows the enable logic for an i/p device at address 1111 0000 on computer system with an 8 bit address & control signals RD & IO/$\overline{M}$

→ The design interface circuitry for an o/p device such as a computer monitor is different.
→ For this tri state buffers are replaced with registers as shown in fig 1.11a.
→ The tri-state buffers are used in i/p device interfaces to make sure that no more than one device writes data to the bus at any time.

AN OUTPUT DEVICE: A) WITH ITS INTERFACE B) THE LOAD LOGIC FOR THE REGISTER

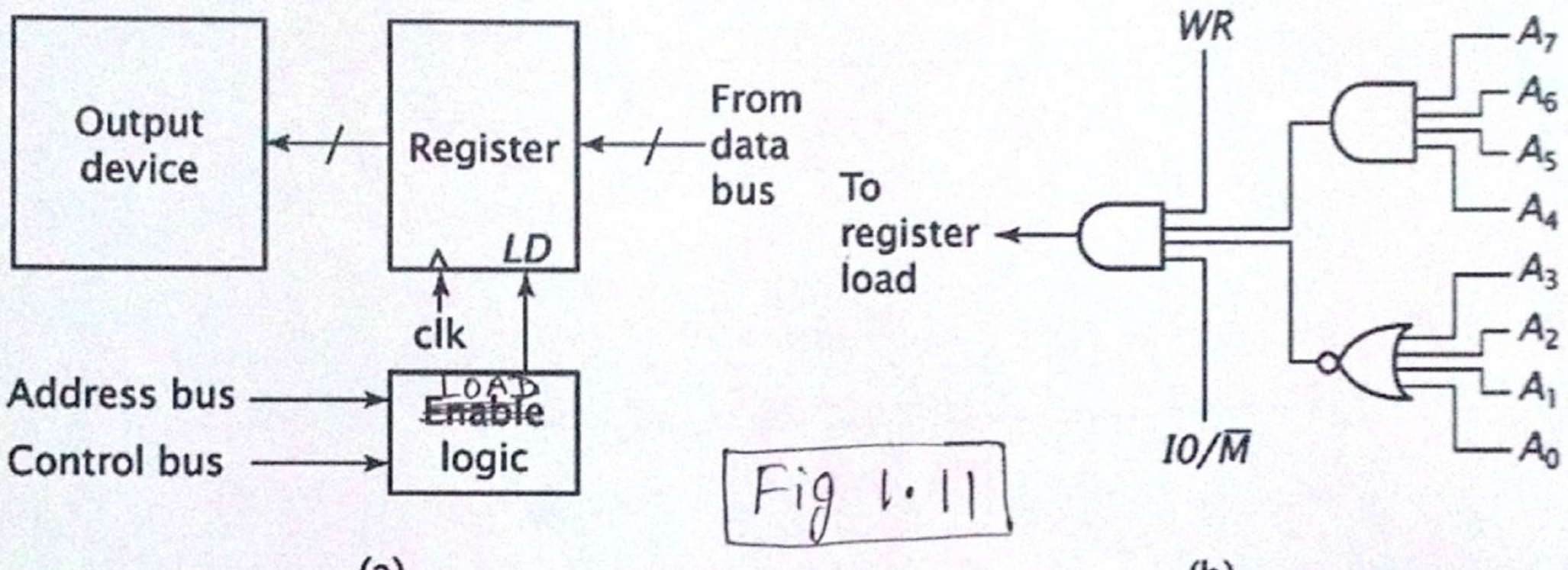


Fig 1.11

→ For o/p devices buffers are not needed. The data can be made available to all output devices; only the device with correct address will read it in.
- When the logic receives correct signals, it asserts the LD signal of the register, causing it to read data from the register at its leisure.
- The logic to generate the load signal for an o/p device at address 1111 0000 is shown in Fig 1.11b

→ Some devices are used for both input & output.
Eg:- Hard disk.
- Such devices requires a combined interface; one for i/p and the other for output.
- The following figure shows a combined I/O interface for address 1111 0000.

A BIDIRECTIONAL INPUT/OUTPUT DEVICE WITH ITS INTERFACE AND ENABLE/LOAD LOGIC

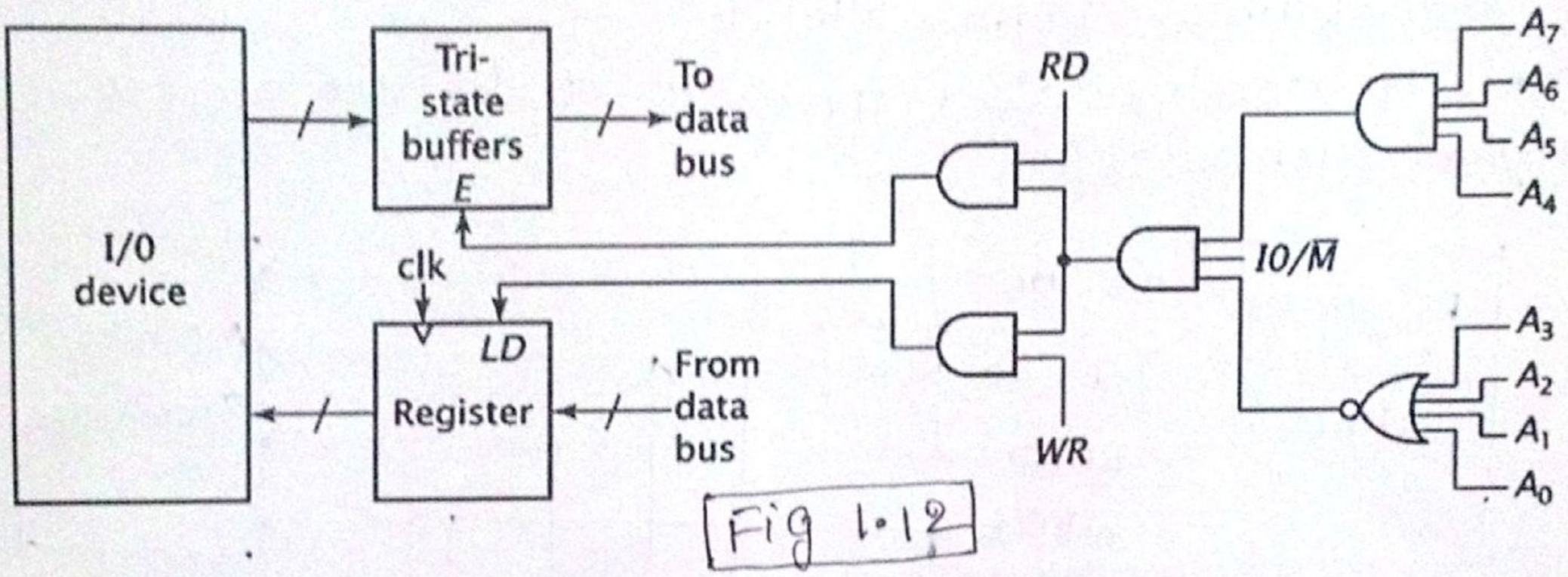


Fig 1.12

- I/o devices are much slower than CPUs and memory. For this reason, they can have timing problems when interacting with the CPU. Most CPUs have a control input signal READY.
- The extra clock cycles generated by having READY set low are called wait states.
- These I/O interfaces are fine for small computers, such as microwave oven controllers, but not suitable for Large Computers.
- Many systems use interrupts so they can perform useful work while waiting for the much slower I/O devices.
- These I/O interfaces are also not suited to large data transfers. Direct Memory Access (DMA) is a method used to by pass the CPU in these transfers, thus performing them much more quickly.

⇒ A Relatively Simple Computer

- Consider a simple computer, that have 8K of ROM starting at address 0, followed by 8K of RAM. It will also have a memory mapped, bidirectional I/O port at address 8000H.

CPU

- for 16 bit addresses - 16 address pins - A_{15} to A_0
- data through D_7 to D_0, data pins.
- 2 control lines READ & WRITE.
- since it uses memory mapped I/O, it does not need a control signal such as IO/$\overline{M}$.

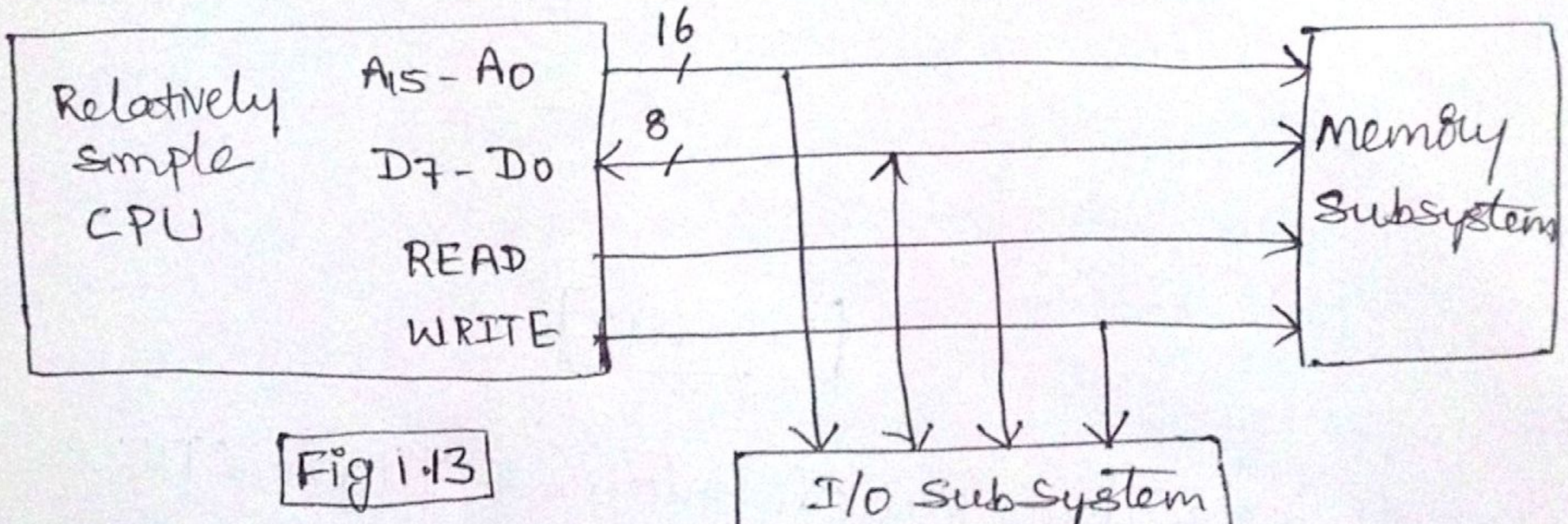


Fig 1.13

A Relatively Simple computer's CPU details only.

Memory Subsystem :-

- ROM contains address in the range 0 to 8K - 1
  0000 0000 0000 0000 to 0001 1111 1111 1111
- The 8K RAM immediately follows the ROM and has address
  8K to 16K - 1
  0010 0000 0000 0000 to 0011 1111 1111 1111
- To access a memory chip, the processor must supply an address used by the chip, as well as the proper control signals.
- ~~To access a memory chip, the processor must supply an address used by the chip~~

- An 8K memory chip has 2^{13} internal memory locations.
- It has 13-bit address input to select one of these locations. (A_{12} to A_0 address bits).
- The remaining 3 bits (A_{15}, A_{14}, A_{13}) will be used to select one (or neither) of the memory.

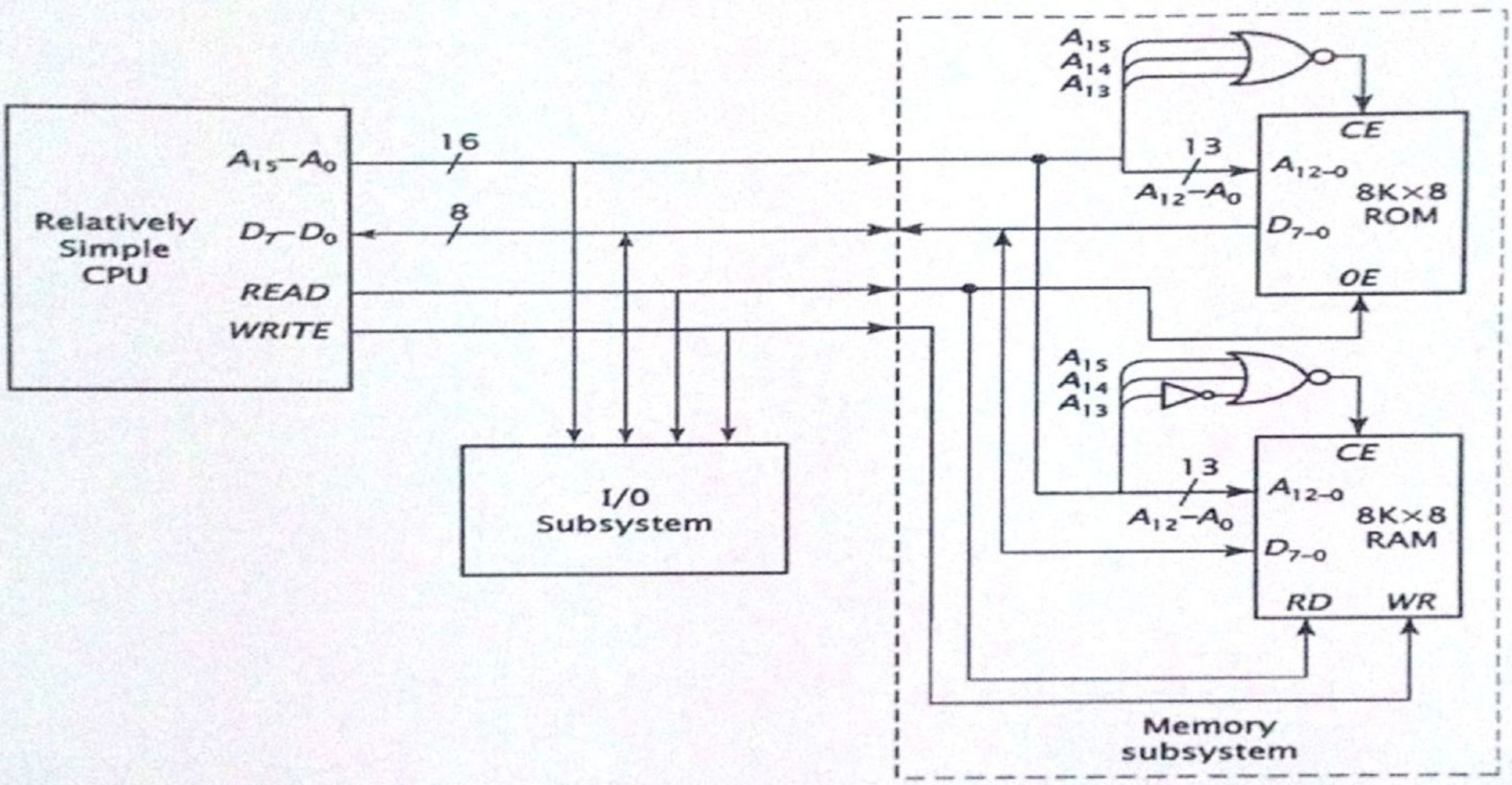


Fig 1.14 A RELATIVELY SIMPLE COMPUTER: MEMORY SUBSYSTEM DETAILS

- The top three address bits of ROM chip are 000 for all addresses.
- Similarly the RAM chip is enabled when $A_{15}A_{14}A_{13} = 001$.
- Read signal is connected to ROM's OE.
- ROM chip outputs data when CE & OE are enabled.
- The RAM has two control inputs, RD and WR. The READ and WRITE signals from the control bus can drive these two signals

→ I/O subsystem :-

- The system specifies one bidirectional I/O port at address 8000H ie 1000 0000 0000 0000 in binary.
- We use the address and the control signals to enable the i/p & o/p interface circuitry for this port.

- We use a register to store data output to the device and tri-state buffers to pass through data to be input from the device.

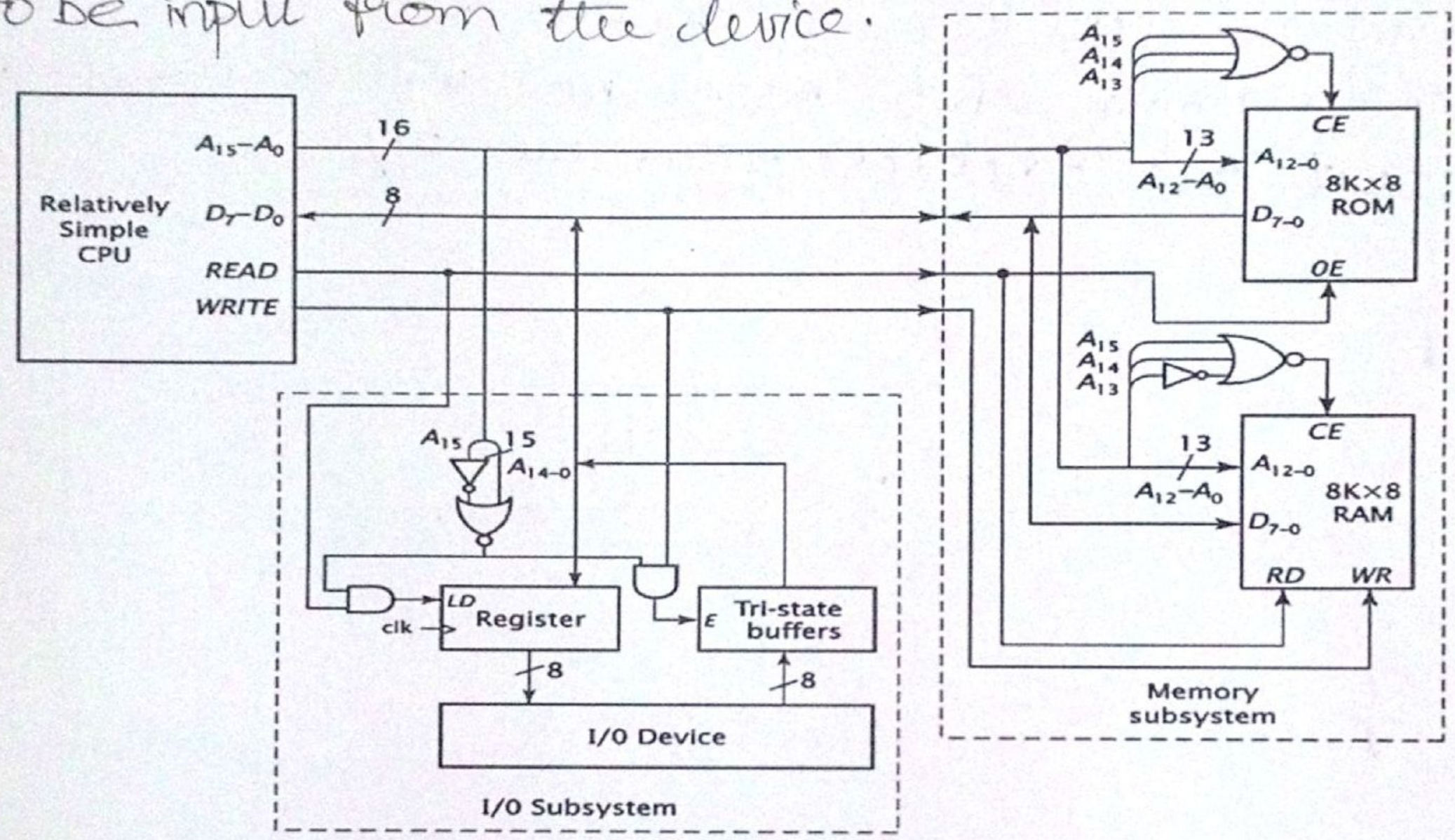
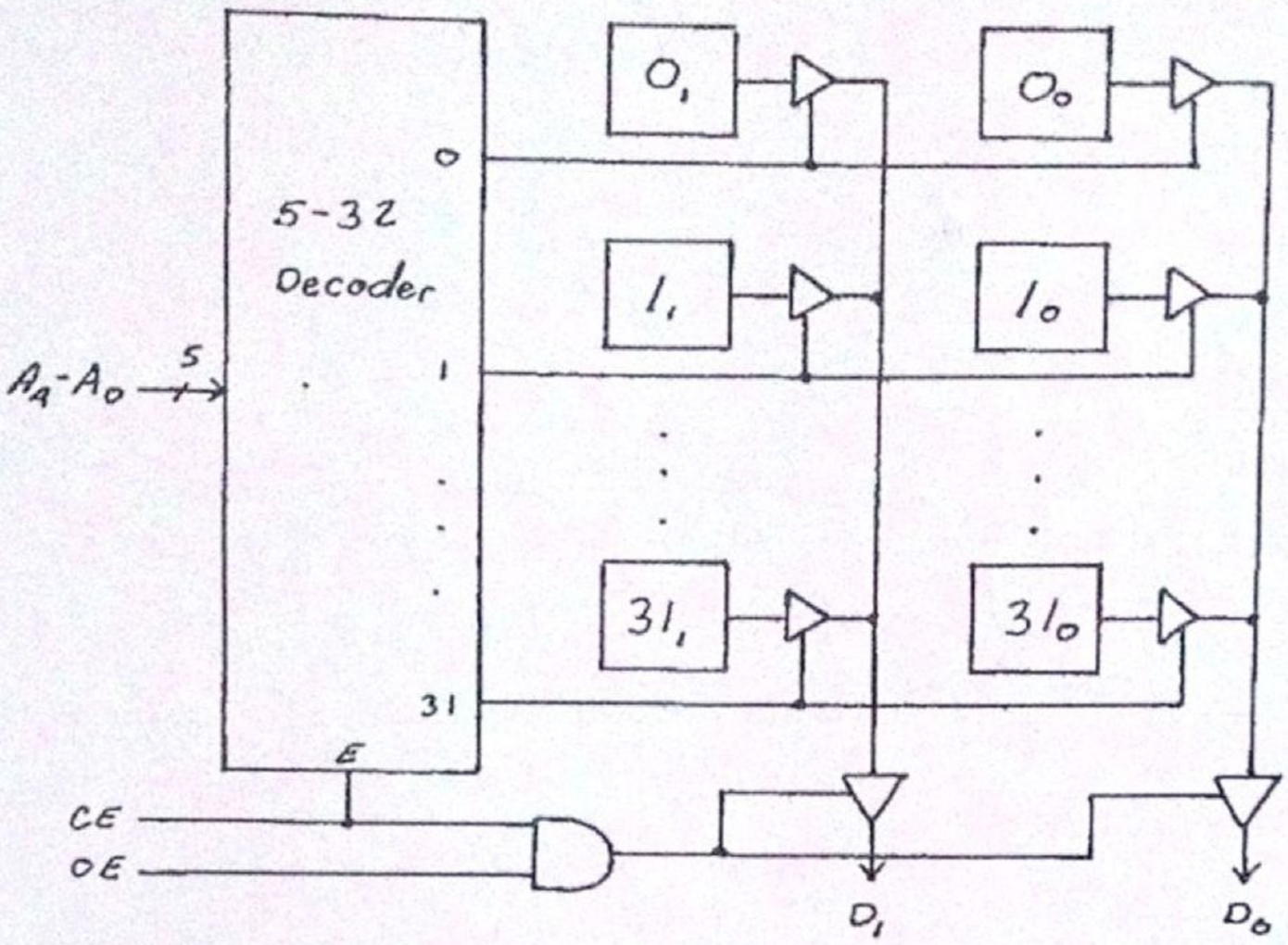


Fig 1.15 A RELATIVELY SIMPLE COMPUTER: FINAL DESIGN

- We need to design the address logic so that it recognizes 8000H.

INTERNAL LINEAR CONFIGURATION OF A 32 X 2 MEMORY CHIP



INTERNAL 2-D CONFIGURATION OF A 32 X 2 MEMORY CHIP