UNIT-I

1. List and explain the functional units of a computer with a neat diagram
2. Explain the computer levels of programming languages
3. a) Explain about instruction formats

   b) Evaluate the arithmetic statement X= A+ (B*C) +D using zero, one, two, three address instructions
4. Explain basic computer organization with a neat diagram
5. Explain different types of primary memory(RAM & ROM)
6. Draw the internal linear and 2-D configuration of 8 X 2 ROM chip. Explain
7. Explain I/O subsystem organization and interfacing
8. a) Explain types of assembly language instructions

   b) Explain various addressing modes
9. Describe a simple computer architecture
10. Describe a simple instruction set architecture

UNIT-II

1. (a) Explain interrupt cycle with flow chart.
   (b) Describe general branch and call/return instructions
2. (a) Draw and explain about the instruction cycle state diagram.
   (b) Describe various arithmetic and logical instruction set operations
3. (a) Explain data transfer and manipulation instructions.
   (b) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.
   (i) What should be the value of the relative address field of the instruction (in decimal)?
   (ii) Determine the relative address value in binary using 12 bits.
   (iii) Determine the binary value in PC after the fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address calculated in part (ii) is equal to the binary value of 500.
4. (a) Explain the different types of addressing modes with examples.
   (b) An instruction is stored at location 300 with its address field at locations 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
   (i) Immediate. (ii) Direct. (iii) Register indirect. (iv) Index with R1 as the index register.
5. Draw the flowchart for Booth's algorithm for multiplication of signed 2's complement numbers and explain with an example.
6. Convert the following numerical expression into reverse polish notation and show the stack operations for evaluating the numerical result: (3+4)*(10*(2+6) +8).
7. What is an addressing mode? A two word instruction is stored in memory at an address designated by symbol. The address field of the instruction (Stored at) is designated by the symbol . The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value . State how Z is calculated from the
8. (a) List the sequence of micro operations needed to execute the following instructions:
   (1) LDA (2) BSA (3) ISZ (4) BUN
   (b) What is an interrupt? Explain about interrupt cycle in detail.
9. List the essential steps required in performing division operation on floating point numbers. Explain them in detail
10. (a) Write short notes on array multiplier.
    (b) Explain the operation of restoring division with flow chart.
11. (a) Explain addition and subtraction algorithm for floating-point data.
    (b) Explain division algorithm for floating-point data.
12. (a) Explain the Booth's algorithm with flow chart.
    (b) Show the contents of register A, E, Q and SC during the process of multiplication of two signed binary numbers 11111 (multiplicand) and 10101 (multiplier).
13. (a) Explain the hardware implementation of unsigned binary multiplication.
    (b) Perform multiplication of unsigned numbers 1101 and 1011.
14. (a) Explain the hardware for signed 2's complement addition and subtraction.
    (b) Perform the following in 2's complement form:
    (i) (+28)10 + (+15)10 (ii) (+28)10 + (-15)10 (iii) (-28)10 + (+15)10(iv) (-28)10 + (-15)10
15. (a) Explain the floating point addition and subtraction with flow chart.
    (b) Show how the following floating point operations are performed (where significants are truncated to 4 decimal digits)
    (i) (0.2255 X 102) X (0.1234 X 101) (ii) (0.8833 X 103) ÷ (0.5555 X 105)
16. (a) Explain the operation of BCD adder with the help of diagram.
    (b)Explain mantissa overflow, mantissa underflow, exponent overflow and exponent underflow.

UNIT-III

1. (a) What are register transfer languages?
   (b) Draw and explain the bus structure for the data transfer between various registers and the common bus.
2. (a) Draw and explain how to construct a bus line using three state buffers.
   (b) How to multiply & divide a number by 2 using shift operations, give an example
3. (a) Explain about arithmetical, logical and shift micro operations.
   (b) Show that the statement A← A + A symbolizes a shift left micro operation.
4. (a) Design a 4 bit combinational circuit decrementer using four full-adder circuits.
   (b) The following transfer statements specify a memory. Explain the memory operation in each case:
      (i) R2← M[AR]
      (ii) M[AR]←R3
      (iii) R5← M[R5]
5. (a) Explain the operation of 4-bit adder-subtractor with example.
   (b) Give hardware implementations to perform logic and shift operations.
6. (a) With a neat sketch explain the 4 bit combinational circuit shifter.
   (b) Starting from an initial value of R = 11011101, determine the sequence of binary values in R after logical shift left, followed by a circular shift-right, followed by a logical shift right and a circular shift-left.
7. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
      (i) How many selection inputs are there in each multiplexer?
      (ii) What size of multiplexers are needed?
      (iii) How many multiplexers are there in the bus?
8. Draw and explain the microprogram sequencer for a control memory
9. Write short notes on the following:
      (a) Hardwired control.
      (b) Microprogrammed control
10. Discuss in detail the design of control unit with block diagram.
11. (a) Explain with the help of diagram the selection of address for control memory.
    (b) Discuss in brief about the applications of microprogramming
12. Explain mapping techniques to convert an operation to a micro routine address in control memory.

UNIT-IV

1. a) Discuss the memory hierarchy in a computer system with regard to speed, size and cost.
   b) What is the need for cache memory? Explain direct mapped cache organization.
2. a) Explain memory hierarchy in detail.
   b) Explain the concept of content addressable memory. How the time for read/write operation is minimized in associative memory?
3. Explain the concept of virtual address and physical address.
4. a) What is cache memory? Explain its operation.
   b) Brief out the hardware organization of associate memory
5. a) With a block diagram explain about associative memory and also explain the match logic, read operation and write operation.
   b) Define RAM and how many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes.
6. The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80% of the memory requests are for read and the remaining 20% are for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.
   (a) What is the average access time of the system considering only memory read cycles?
   (b) What is the average access time of the system for both read and write requests?
7. a) The access time of the main memory is 700 ns and the access time of the cache memory is 100 ns. The hit ratio for the read access is only 0.8. What is the average access time of the system considering only memory read cycles?
   b) Explain memory address map.
8. To construct a memory unit with capacity of 4096 bytes, only 128 x 8 RAM chips are available, how many of them are used to get the memory capacity. If so how many address lines are needed to access the memory and how many lines are needed to access each chip
9. a) Discuss the various I/O interfacing techniques.
   b) Discuss the programmed I/O.
10. With a neat diagram, describe DMA transfer in a computer system
11. What is the advantage of priority interrupt over non priority interrupt? Explain the use of mask register.
12. a) What is DMA? Explain the transfer of data from memory to I/O device with the help of a flow chart.
    b) Explain the limitations in programmed I/O and interrupt driven I/O.
13. What is an I/O interface? Describe methods to implement the same with two examples
14. a) Explain the methods of priority resolution for interrupts.
    b) Explain handshaking in asynchronous data transfer.
15. Explain the interrupt priority system using daisy chain.
16. a) Explain in detail the strobe control method of asynchronous data transfer.
    b) Draw block diagram of typical daisy-chain priority interrupt scheme and explain its operation.

UNIT-V

1. (a) What is pipeline? Explain.
   (b) Explain arithmetic pipeline.
2. A nonpipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved
3. Explain the following with neat sketches:
   (a) Parallel processing.
   (b) Arithmetic pipeline.
4. (a) What is pipeline? Explain space-time diagram for pipeline.
   (b) Explain pipeline for floating point addition and subtraction.
5. Classify the pipeline processors and explain them in detail
6. What is the Flynn's classification of the computer system? Explain in detail.
7. (a) Explain serial arbitration logic.
   (b) Give short notes on the system bus.
8. (a) Give a short note on SISD and SIMD multiprocessing.
   (b) List out the types of multiprocessing. Explain.
9. What are the various physical forms available for establishing an interconnection network? Explain
10. (a) Explain the hardware organization for four stage instruction pipeline.
    (b) What is a data hazard?
11. Discuss in detail about inter processor communication and synchronization
12. (a) Compare communication costs in multicomputer and multiprocessor systems.
    (b) Explain about Amdahl's law.
13. (a) Explain the functioning of omega switching network with a neat sketch.
    (b) In 8 x 8 omega switching network how many stages are there and in each stage how many switches are there.
14. (a) Explain the process of arithmetic pipelining with an example.
    (b) Explain the terms data dependencies, hardware interlock and operand forwarding techniques
15. (a) What do you mean by bus arbitration?
    (b) Explain the serial arbitration technique with the help of a neat diagram. State
16. advantages and disadvantages
17. (a) Explain with the help of a neat sketch how a time shared bus inter connection system for multiple processors provide a common communication path connecting all of the functional units.
    (b) Draw the sketch and explain the multiprocessor with unidirectional buses.
18. (a) Explain the inter processor communication using message passing.
    (b) How does message transfer system function?
19. (a) Explain the Interprocessor communication.
    (b) Write in detail about Interprocessor arbitration.
20. (a) Differentiate tightly coupled and loosely coupled multiprocessors according to hardware.
    (b) Explain the functioning of omega switching network with a neat sketch.