

COMPUTER ORGANIZATION AND ARCHITECTURE

ASSIGNMENT –2

1. Consider the instruction formats of the basic computer. For each of the following 16-bit instructions, give the equivalent four-digit hexadecimal code and explain in your own words what it is that the instruction is going to perform.
 - a. 0001 0000 0010 0100
 - b. 1011 0001 0010 0100
 - c. 0111 0000 0010 0000
2. Write a program to evaluate the arithmetic statement:
$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$
 - a. Using a general register computer with three address instructions.
 - b. Using a general register computer with two address instructions.
 - c. Using an accumulator type computer with one address instructions.
 - d. Using a stack organized computer with zero-address operation instructions.
3. An instruction at address 021 in the basic computer has I = 0, an operation code of the AND instruction, and an address part equal to 083 (all numbers are in hexadecimal). The memory word at address 083 contains the operand B8F2 and the content of AC is A937. Go over the instruction cycle and determine the contents of the following registers at the end of the execute phase: PC, AR, DR, AC, and IR. Repeat the problem six more times starting with an operation code of another memory-reference instruction.
4. The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.
 - a. What is the instruction that will be fetched and executed next?
 - b. Show the binary operation that will be performed in the AC when the instruction is executed.
 - c. Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the values of E, I, and the sequence counter SC in binary at the end of the instruction cycle.
5. Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result.
$$(3 + 4) * [10 * (2 + 6) + 8]$$
6. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word.
7. A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.
 - a. What should be the value of the relative address field of the instruction (in decimal)?
 - b. Determine the relative address value in binary using 12 bits. (Why must the number be in 2's complement?)
 - c. Determine the binary value in PC after the fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address calculated in part (b) is equal to the binary value of 500.
8. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R 1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register.

"Education is not preparation for life; education is life itself."

~John Dewey

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