COMPUTER ORGANIZATION AND ARCHITECTURE

ASSIGNMENT –3

1. Perform the arithmetic operations below with binary numbers and with negative numbers in signed 2's complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position.
   a. (+35) + (+40)
   b. (-35) + (-40)
   c. (-35) - (+40)

2. Show the contents of registers E, A, Q, and SC during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). The signs are not included.

3. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers. The multiplicand in both cases is + 15.
   a. (+ 15) * (+ 13) b. (+ 15) * (- 13)

4. Show the contents of registers E, A, Q, and SC during the process of division of
   (a) 10100011 by 1011; (b) 00001111 by 0011. (Use a dividend of eight bits.)

5. Show the content of registers A, B, Q, and SC during the decimal multiplication of
   (a) 470 x 152 and (b) 999 x 199. Assume three-digit registers and take the second number as the multiplier.

6. Show the content of registers A, E, Q, and SC during the decimal division of 1680/32. Assume two-digit registers.