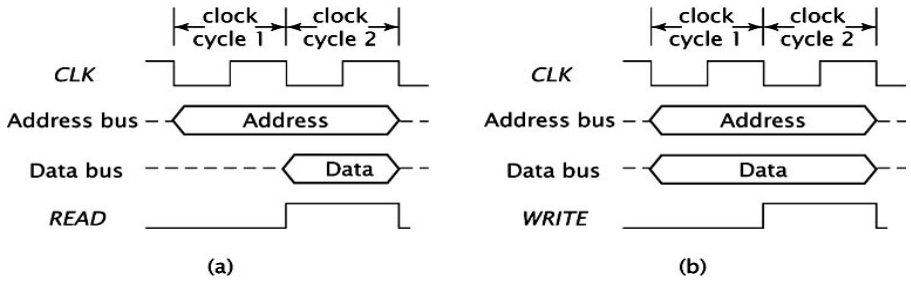
UNIT-I

1. **What is bus; list the different types of buses with its function.**

A group of lines that serves as a connecting path for several devices is called a bus;

TYPES: ADDRESS BUS, DATA BUS, CONTROL BUS

2. **Draw the timing diagrams for memory read and memory write operations.**



3. **List the different types of memory chips.**

RAM: Random Access Memory ROM: Read Only Memory

4. **List different registers that CPU contains.**

Instruction Register, Program Counter, Address Register, Data Register

5. **What are different types of ROM chips?**

Masked ROM, PROM, EPROM, EEPROM

6. **What is a compiler?**

A system software program called a compiler translates the high-level language program into a suitable machine language program containing instructions such as the Add and Load instructions.

7. **List out the types of assembly language instruction based on the type of operations they perform**

DATA TRANSFER INSTRUCTIONS

DATA MANIPULATION INSTRUCTIONS

PROGRAM CONTROL INSTRUCTIONS

8. **Differentiate between computer organization and architecture**

Computer architecture refers to those parameters of a computer system that are visible to a programmer or those parameters that have a direct impact on the logical execution of a program. Examples of architectural attributes include the instruction set, the number of bits used to represent different data types, I/O mechanisms, and techniques for addressing memory.

Computer organization refers to the operational units and their interconnections that realize the architectural specifications. Examples of organizational attributes include those hardware details transparent to the programmer, such as control signals, interfaces between the computer and peripherals, and the memory technology used.

9. List any five assembly language instructions

STORE, LOAD, ADD, MUL, DIV, HALT

10. What is big endian and little endian format.

The name big endian is used when lower byte addresses are used for the more significant of the word.The name little endian is used for the less significant bytes of the word.

11. What is the function of CU?

The control unit acts as the nerve center that coordinates all the computer operations. It issues timing signals that governs the data transfer.

12. What are basic operations of a computer?

The basic operations are READ and WRITE.

13. What is byte addressable memory?

The assignment of successive addresses to successive byte locations in the memory is called byte addressable memory.

14. What is assembly language?

A complete set of symbolic names and rules for the use of machines constitute a programming language, generally referred to as an assembly language.

15. What is the advantage of non restoring over restoring division?

Non restoring division avoids the need for restoring the contents of register after an successful subtraction.

16. What is booting?

When the power is turned on the OS has to be loaded into the main memory ,which takes place as part of a process called booting. To initiate booting a tiny part of main memory is implemented as a nonvolatile ROM.

17. What is application software? Give example.

Application programs are usually written in a high level programming language, in which the programmer specifies mathematical or text processing operations. These operations are described in a format that is independent of the particular computer used to execute the program.

18. **Compare Static RAM and Dynamic RAM**

	PARAMETER	STATIC RAM	DYNAMIC RAM
1.	Cell Type	Flip Flop Cell	Capacitor Storage Cell
2.	Speed	Fast	Slow
3.	Refreshing	Not Required	Required
4.	Density	Less	More
5.	Cost	More	Less

19. How many 128 X 8 RAM chips will be needed to provide capacity of 1024 bytes

1024 / 128 = 8 chips

20. What is the maximum size of the address space generated in a processor with has 32 bit address?

The maximum size of the address space generated in a processor with has 32 bit address = 232 = 4 Giga Locations.

21. What will be the number of address and data lines required for a 512K X 8 memory system

No. of address lines = 19

No. of data lines = 8

22. What is byte addressable memory?

The assignment of successive addresses to successive byte locations in the memory is called byte addressable memory.

UNIT-II

23. What are the steps in executing a program?

1.Fetch
2.Decode
3.Execute
4.Store

24. List any five register reference instructions

CLA	AC←0	CLEAR ACCUMULATOR
CLE	E←0	CLEAR E
CMA	AC←$\overline{AC}$	COMPLEMENT AC
CME	E←$\overline{E}$	COMPLEMENT E
INC	AC←AC+1	INCREMENT AC

25. Give the microoperations for execution of LDA instruction

LDA : Load to AC

This instruction transfers the memory word specified by the effective address to AC. The microoperations needed to execute this instruction are

D2 T4: DR ← M[AR]

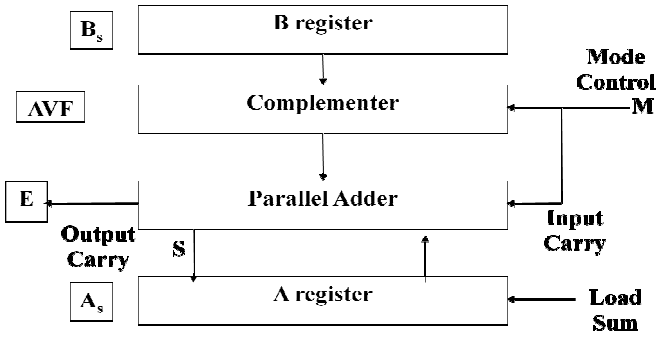
D2 T5: AC ← DR, SC ← 0

26. List types of interrupts

Three types of interrupts:

1. External interrupts
2. Internal interrupts
3. Software interrupts

27. Draw the hardware implementation for addition and subtraction with signed magnitude data



28. Consider the instruction formats of the basic computer 0001 0000 0010 0100. what is the instruction going to perform

0001 0000 0010 0100➔ADD content of M[024] to AC ➔ADD 024

29. List any five system registers.

Instruction Register, Program Register, Data Register, Address Resister, Accumulator

30. What is a bias exponent representation?

In Bias exponent representation, the sign bit is removed from being a separate entity. The bias is a positive number that is added to each exponent as the floating-point number is formed, so that internally all exponents are positive.

31. List any three program control instructions.

Branch	BR
Jump	JMP
Skip	SKP
Call	CALL
Return	RET
Compare	CMP
Test	TST

32. What are the registers generally contained in the processor?

MAR-Memory Address Register MDR-Memory Data Register

IR-Instruction Register R0-Rn-General purpose Registers

PC-Program Counter

33. Define interrupt and ISR?

An interrupt is a request from an I/O device for service by the processor. The processor provides the requested service by executing the interrupt service routine

34. Convert the following numerical arithmetic expression into reverse Polish notation

(3 + 4)*[10*(2 + 6) + 8]

3 4 + 10 2 6 + * 8 + *

STACK											
						6					
					2	2	8		8		
		4		10	10	10	10	80	80	88	
	3	3	7	7	7	7	7	7	7	7	616

OPERATION	PUSH(3)	PUSH(4)	ADD	PUSH(10)	PUSH(2)	PUSH(6)	ADD	MUL	PUSH(8)	ADD	MUL

35. What is branch target?

As a result of branch instructions, the processor fetches and executes the instruction at a new address called branch target, instead of the instruction at the location that follows the branch instruction in sequential address order

36. Define various addressing modes.

The various addressing modes are

1. Absolute addressing mode 2.Register addressing mode 3.Indirect addressing mode
4.Index addressing mode 5.Immediate addressing mode 6.Relative addressing mode
7. Autoincrement addressing mode 8.Autodecrement addressing mode

UNIT-III

37. Define processor clock.

Processor clock is defined as the time periods in which all operations and data transfers within the processor take place

38. What are the two approaches used for generating the control signals in proper sequence?

Hardwired control Microprogrammed control

39. Explain hardwired control.

The control hardwire can be viewed as a state machine that changes from one state to another in every clock cycle, depending on the contents of the instruction register, the condition codes, and the external inputs. The outputs of the state machine are the control signals. The sequence of operations carried out by this machine is determined by the wiring of the logic elements, hence the name "hardwired".

40. What are the features of the hardwired control?

A controller that uses this approach can operate at high speed. It has little flexibility and the complexity of the instruction set it can implement is limited.

41. What is microprogrammed control?

Microprogrammed control is a scheme in which control signals are generated by a program similar to machine language programs.

42. What is control word?

A control word is a word whose individual bits represent the various control signals.

43. Define microroutine and microinstruction.

A sequence of control words corresponding to the control sequence of a machine instruction constitutes the microroutine for that instruction, and the individual control words in this microroutine are referred to as microinstructions.

44. What is control store?

The microroutines for all instructions in the instruction set of a computer are stored in a special memory called the control store.

45. What is vertical organization and horizontal organization?

Highly encoded schemes that use compact codes to specify only a small number of control functions in each microinstruction are referred to as a vertical organization. On the other hand, the minimally encoded scheme in which many resources can be controlled with a single microinstruction is called a horizontal organization

46. **Define Memory Access Time and Memory Cycle Time**

Memory Access Time – is the time interval between the initiation and completion of Read or Write Operation

Memory Cycle Time – is the minimum Time interval required between initiation of Two successive memory operation.

UNIT-IV

47. What are different modes of transfer

Programmed I/O

Interrupted Initiated I/O

Direct Memory Access(DMA)

48. What is the disadvantage of programmed I/O

In the programmed I/O method, the CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer. This is a time-consuming process since it keeps the processor busy needlessly.

49. What is cache memory?

The small and fast RAM units are called as caches. When the execution of an instruction calls for data located in the main memory, the data are fetched and a copy is placed in the cache. Later if the same data is required it is read directly from the cache.

50. What are the cache write protocols? Briefly explain.

There are two types of cache write protocols

i) Write Through: The Cache locations and the main memory location are updated simultaneously.

ii) Write Back: Here the cache location is updated and it is marked dirty. The main memory location is updated later when the block is marked dirty is to be removed from the cache to make room for a new block.

51. What are the cache mapping algorithms?

1. Direct Mapping
2. Associative Cache
3. Set Associative Cache

52. An application program in a computer with cache uses 1400 instruction fetch from cache and 100 from main memory. What is hit ratio?

Hit Ratio = No. of Instruction fetch from cache / Total no. of instructions = 1400 / 1500 = 93.333%

53. What is the use of cache memory?

The use of cache memories solves the memory access problem. In particular, when a cache is included on the same chip as the processor, access time to the cache is usually the same as the time needed to perform other basic operations inside the processor. This makes it possible to divide instruction fetching and processing into steps that are more or less equal in duration. Each of these steps is performed by a different pipeline stages, and the clock period is chosen to correspond to the longest one.

54. Define memory access time?

The time required to access one word is called the memory access time.

or

It is the time that elapses between the initiation of an operation and the completion of that operation.

55. Define memory cycle time?

It is the minimum time delay required between the initiation of two successive memory operations.

Eg. The time between two successive read operations.

56. What are the Characteristics of SRAMs?

SRAMs are fast. They are volatile. They are of high cost. Less density.

57. .What are the Characteristics of DRAMs?

Low cost.

High density.

Refresh circuitry is needed.

58. What is locality of reference?

Analysis of programs shows that many instructions in localized areas of the program are executed repeatedly during some time period., and the remainder of the program is accessed relatively infrequently. This is referred to as locality of reference. This property leads to the effectiveness of cache mechanism.

59. What are the two ways in which the system using cache can proceed for a write operation?

Write through protocol technique.

Write-back or copy back protocol technique

60. What is replacement algorithm?

When the cache is full and a memory word that is not in the cache is referenced, the cache control hardware must decide which block should be removed to create space for the new block that contains the reference word .The collection of rules for making this decision constitutes the replacement algorithm.

61. What is page frame?

An area in the main memory that can hold one page is called as page frame.

62. What is DMA?

Transfer of a block of data directly between an external device and main memory, without continuous intervention by the processor is called DMA.

63. What is DMA controller?

DMA transfers are performed by a control circuit that is part of the I/O device interface. This circuit is known as DMA controller.

64. What is cycle stealing?

The processor originates most memory access cycles and the DMA controller can be said to steal memory cycles from the processor. This technique is known as cycle stealing.

65. What is bus arbitration?

It is the process by which the next device becomes the bus master is selected and bus master ship is transferred to it.

66. What is a Priority Interrupt?

A priority interrupt is an interrupt that establishes a priority over the various sources to determine which condition is to be serviced first when two or more requests arrive simultaneously.

67. What do you mean by synchronous and asynchronous data transfer

The internal operations in a digital system are synchronized by means of clock pulses supplied by a common pulse generator. If the registers in the interface share a common clock with the CPU registers, the transfer between the two units is said to be synchronous.

In most cases, the internal timing in each unit is independent from the other in that each uses its own private clock for internal registers. In that case, the two units are said to be asynchronous to each other.

UNIT-V

68. Define pipelining

Pipelining is an implementation technique where multiple instructions are overlapped in execution. The computer pipeline is divided in stages. Each stage completes a part of an instruction in parallel.

OR

Pipelining is a technique of decomposing a sequential process into sub operations, with each sub process being executed in a special dedicated segment that operates concurrently with all other segments

69. Name the four steps in instruction pipelining.

1. FI: Fetch an instruction from memory
2. DA: Decode the instruction and calculate the effective address of the operand
3. FO: Fetch the operand
4. EX: Execute the operation

70. Define throughput

The amount of processing that can be accomplished during a given interval of time

71. What are the four major groups of Flynn's classification of computers

Flynn's Computer classification:

- Single instruction stream, single data stream – SISD
- Single instruction stream, multiple data stream – SIMD
- Multiple instruction stream, single data stream – MISD
- Multiple instruction stream, multiple data stream – MIMD

72. Give the types of multiprocessors that are classified by the way their memory is organized

A multiprocessor system with common shared memory is classified as a **shared memory or tightly coupled multiprocessor**.

An alternative model of microprocessor is the **distributed-memory or loosely coupled system**. Each processor element in a loosely coupled system has its own private local memory.

73. Draw the space-time diagram for a four segment pipeline with six tasks

Space-time diagram for pipeline.

Segment:	1	2	3	4	5	6	7	8	9	→ Clock cycles
1	T_1	T_2	T_3	T_4	T_5	T_6				
2		T_1	T_2	T_3	T_4	T_5	T_6			
3			T_1	T_2	T_3	T_4	T_5	T_6		
4				T_1	T_2	T_3	T_4	T_5	T_6	

74. What are the four segments in Four- segment instruction pipeline

1. FI: Fetch an instruction from memory
2. DA:Decode the instruction and calculate the effective address of the operand
3. FO: Fetch the operand
4. EX: Execute the operation

75. Define the term hardware interlocks

Hardware interlocks are circuits that detect instructions whose source operands are destinations of prior instructions. Detection causes the hardware to insert the required delays without altering the program sequence.

76. Define a System bus

A bus that connects major components in a multiprocessor system, such as CPUs, IOPs, and memory, is called a **system bus**.

77. What is delayed branching?

A technique called delayed branching can minimize the penalty incurred as a result of conditional branch instructions. The idea is simple. The instructions in the delay slots are always fetched. Therefore, we would like to arrange for them to be fully executed whether or not the branch is taken. The objective is to be able to place useful instructions in these slots. If no useful instructions can be placed in the delay slots, these slots must be filled with NOP instructions.

78. What is synchronous bus?

In this, all devices derive timing information from a common clock line.

79. What is asynchronous bus?

In this, all devices do not derive timing information from a common clock line. It uses handshake between the master and the slave.

80. What are different dynamic arbitration algorithms

Time slice algorithm
Polling
Least recently used (LRU) algorithm
First-come, first-serve
Rotating daisy-chain

81. **What is communication**

Communication refers to the exchange of data between different processes. For example, parameters passed to a procedure in a different processor constitute interprocessor communication.

82. **What is synchronization**

Synchronization refers to the special case where the data used to communicate between processors is control information. Synchronization is needed to enforce the correct sequence of processes and to ensure mutually exclusive access to shared writable data.

83. Define critical section

A **critical section** is a program sequence that, once begun, must complete execution before another processor accesses the same shared resource.

84. What is a semaphore

A binary variable called a **semaphore** is often used to indicate whether or not a processor is executing a critical section. A semaphore is a software controlled flag that is stored in a memory location that all processors can access.

85. **What are hazards? Write its types.**

There are situations in pipelining when the next instruction cannot be executed inthe following clock cycle. These events are called hazards, and there are three differenttypes.

1. Structural Hazards
2. Data Hazards
3. Control Hazards

86. **What is meant by forwarding?**

Forwarding, also called bypassing, is a method of resolving a data hazard byretrieving the missing data element from internal buffers rather than waiting for it toarrive from programmer visible registers or memory.

87. **What is pipeline stall?**

Pipeline stall, also called bubble, is a stall initiated in order to resolve a hazard