COMPUTER ORGANIZATION AND ARCHITECTURE

1. Which register store the address of next instruction to be executed?

   A) **PC** B) AC C) SP D) NONE

2. How many bits are required to address the 128 words of memory?

   A) **7** B) 8 C) 9 D) NONE

3. _____ is the volatile memory.

   A) **RAM** B) ROM C) AUXILARY D) NONE

4. C is the _____ type of language.

   A) **High** B) Low C) machine D) None

5. Machine language consists of _____

   A) **binary values** B) Decimal values C) Alphabets D) Symbols

6. _____ is required for high level languages to translate into machine language.

   A) **compiler** B) assembler C) a & b D) None

7. A collection of lines that connects several devices is called _____

   A) **Bus** b) port c) cable d) link

8. _____ is the first phase of instruction cycle

   A) **fetch** B) decode C) execute D) interrupt

9. CPU never reads data from _____bus

   A) **address bus** B) data bus C) control bus D) all the above

10. ____ is the cache memory .

    A) **SRAM** B) DRAM C) ROM D) NONE

11. JAVA is the _____ type of language.

    A) **High** B) Low C) machine D) None

12. _____ is the non - volatile memory.

    A) RAM B) **ROM** C) Registers D) NONE

13. Which register store the top of the stack.

    A) PC B) AC C) **SP** D) NONE

14. Operation of memory transfer are:

    A) Read B) Write C) **Both** D) None

15. System bus contains___

    A) address bus B) data bus C) control bus D) **ALL**

16. In sign magnitude representation, which bit represent the sign of the binary number.

    A) LSB B) **MSB** C) A & B D) NONE

17. In shl , zero is inserted from_____ bit position .

    A) **LSB** B) MSB C) A & B D) NONE

18. Execution of memory reference instructions begins at ___ timing signal

A) T3 B) T2 C) T1 D) **T4**

19. LD @ADR designates which addressing mode___

A) direct B) **indirect** C) relative D) indexed

20. shr 101010 =_____

A) **010101** B) 110101 C) 110010 D) 011011

21. ashr 101010=

A) 010101 B) **110101** C) 110010 D) 011011

22. The micro operation M[AR] ←AC, SC← 0 specifies _____ instruction

A) **STA** B) LDA C)CLA D) ADD

23. For a memory unit with 4096 words we need how many address bits?

A) 6 B) 15 C) **12** D) 8

24. Which one of the following is data transfer instruction

A) **LD** B)ADD C) INC D)CLR

25. Booth's algorithm is used to multiply binary integers in _____ representation.

A) Signed magnitude B) Signed 1's complement C) **Signed2's complement** D) None

26. Postfix notation of (A+B)*C is

A). AB+*C B). AB*+C C). ABC+* D). **AB+C***

27. In floating point division, exponents should be _____ .

A)added B) **subtracted** C) multiply D) divide

28. The binary information of source register chosen by:

A) Demultiplexer B) **Multiplexer** C) Both D) None

29. A control unit whose binary control variables are stored in memory is called a __ control unit.

A) Hard-wired B) **Micro-programmed** C) Soft-wired D) Macro-programmed

30. CAR stands for_____

A) **Control Address Register** B) Control Add Register C) Content Address Register D)None

31. A group of bits that tell the computer to perform a specific operation is known as

(A) **Instruction code** (B) Micro-operation (C) Accumulator (D) Register

32. A microprogram sequencer

(A) **generates the address of next micro instruction to be executed.**

(B) generates the control signals to execute a microinstruction.

(C) sequentially averages all microinstructions in the control memory.

(D) enables the efficient handling of a micro program subroutine

33. A register capable of shifting its binary information either to the right or the left is called a

(A) parallel register. (B) serial register. (C) **shift register.** (D) storage register.

34. Logic X-OR operation of (4ACO)H& (B53F)H results _____.

A. AACB B. 0000 C. **FFFF** D. ABCD

35. RTL stands for:

a. Random transfer language **b. Register transfer language**

c. Arithmetic transfer language d. All of these

36. The register that includes the address of the memory unit is termed as the ____:

a. MAR b. PC c. IR d. None of these

37. Micro operation to transfer data from R2 to R1 is shown as:

a. R1→R2 **b. R1←R2** c. Both d. None

38. Which operation is extremely useful in serial transfer of data:

a. Logical micro operation b. Arithmetic micro operation c. Shift micro operation d. None of these

39. In 3 state gate third position termed as high impedance state which acts as:

a. Open circuit b. Close circuit c. None of these d. All of above

40. Which operation refer bitwise manipulation of contents of register:

a. Logical micro operation b. Arithmetic micro operation c. Shift micro operation d. None of these

41. Which language specifies a digital system which uses specified notation:

A) Register transfer B) Arithmetic C) Logical D) All of these

42. In which shift is used to divide a signed number by two:

A) Logical right-shift B) **Arithmetic right shift**

C) Logical left shift D) Arithmetic left shift

43. A computer's memory is composed of 8K words of 32 bits each. How many bits are required for memory address if the smallest addressable memory unit is a word?

a. 13 b. 8 c. 10 d. 6

44. A computer's memory is composed of 4K words of 32 bits each. How many total bits in memory?

a. 12800 b. 1280000 c. 1310720 **d. 131072**

45. A computer's memory is composed of 8K words of 32 bits each, and a byte is 8 bits. How many bytes does this memory contain?

a. 8K **b. 32K** c. 16K d. 4K

46. A computer's memory is composed of 8K words of 32 bits each, and the smallest addressable memory unit is an 8 bit byte. How many bits will be required for the memory address?

a. 12 **b. 15** c. 13 d. 10

47. Cache memory refers to

a. cheap memory that can be plugged into the mother board to expand main memory

b. fast memory present on the processor chip that is used to store recently accessed data

c. a reserved portion of main memory used to save important data

d. a special area of memory on the chip that is used to save frequently used constants

48. Which of the following is lowest in memory hierarchy?

(A) Cache memory (B) **Secondary memory** (C) Registers (D) RAM

49. In a vectored interrupt.

(A) the branch address is assigned to a fixed location in memory.

(B) the interrupting source supplies the branch information to the processor through an interrupt vector.

(C) the branch address is obtained from a register in the processor

(D) none of the above

50. The circuit used to store one bit of data is known as

(A) Encoder (B) OR gate (C) **Flip Flop** (D) Decoder

51. Write Through technique is used in which memory for updating the data

(A) Virtual memory (B) Main memory (C) Auxiliary memory (D) **Cache memory**

52. Cache memory works on the principle of

(A) Locality of data (B) Locality of memory

(C) **Locality of reference** (D) Locality of reference & memory

53. Memory unit accessed by content is called

(A) Read only memory (B) Programmable Memory

(C) Virtual Memory (D) **Associative Memory**

54. 'Aging registers' are

(A) **Counters which indicate how long ago their associated pages have been referenced.**

(B) Registers which keep track of when the program was last accessed.

(C) Counters to keep track of last accessed instruction.

(D) Counters to keep track of the latest data structures referred.

55. An address in main memory is called

(A) **Physical address** (B) Logical address (C) Memory address (D) Word address

56. ____organization refers to a computer system capable of processing several programs at the same time

A) SISD B) SIMD C) MISD D) **MIMD**

57. SISD represents the organization of single computer containing ----------

A) Control unit B) processor unit C) memory unit D) **all**

58. Which is a type of microprocessor that is designed with limited number of instructions:

a. CPU **b. RISC** c. ALU d. MUX

59. Which unit is a pipeline system helps in speeding up processing over a non pipeline system:

a. CPU b. RISC c. ALU d. MUX

60. SIMD stands for:

a. System instruction multiple data **b. Single instruction multiple data**

c. Symmetric instruction multiple data d. Scale instruction multiple data

61. MIMD stands for:

a. Multiple input multiple data b. Memory input multiple data

c. Multiple instruction multiple data d. Memory instruction multiple data

62. Which is a method of decomposing a sequential process into sub operations:

a. Pipeline b. CISC c. RISC d. Database

63. Which is used to speed-up the processing:

a. Pipeline b. Vector processing **c. Both** d. None

64. Which processor is a peripheral device attached to a computer so that the performance of a computer can be improved for numerical computations:

a. Attached array processor b. SIMD array processor c. Both d. None

65. Which types of register holds a single vector containing at least two read ports and one write ports:

a. Data system b. Data base c. Memory **d. Vector register**

66. Which control refers to the track of the address of instructions:

a. Data control b. Register control **c. Program control** d. None of these

67. SDRAM stands for:

a. System dynamic random access memory **b. Synchronous dynamic random access memory** c. Both d. None

68. Which operation are associated with serial transfer of data:

a. Logical micro operation b. Arithmetic micro operation **c. Shift micro operation** d. None of these

69. The contents of the program counter is the _____ of the instruction to be run:

a. Data **b. Address** c. Counter d. None of these

70. A group of 4 binary bits is called:

    a. Nibble b. Byte c. Decimal d. Digit

71. Which is a method of decomposing a sequential process into sub operations:

    a. Pipeline b. CISC c. RISC d. Database

72. Which device can be thought of as transducers which can sense physical effects and convert them into machine-tractable data:

    a. Storage devices b. **Peripheral devices** c. Both d. None

73. In _____ addressing technique separate address space is used for both memory and I/O device:

    a. Memory-mapped I/O b. **Isolated I/O** c. Both a & b d. None of these

74. _____operations are the results of I/O operations that are written in the computer program:

    a. **Programmed I/O** b. DMA c. Handshaking d. Strobe

75. Which technique is used that identifies the highest priority resource by means of software:

    a. Daisy chaining b. **Polling** c. Priority d. Chaining

76. VAD stands for:

    a. **Vector address** b. Symbol address c. Link address d. None of these

77. ____interrupt method uses a register whose bits are set separately by interrupt signal for each device:

    a. **Parallel priority interrupt** b.Serial priority interrupt c.Both a & b d. None of these

78. Which is used to decentralize the decision to avail greater flexibility to the system that makes processor or microprocessor in a very short:

    a. **Arbitration** b. Centralized c. Both a & b d. None of these

79. ___ is basically sequence of instructions with a clear indication of beginning and end for updating shared variables

    a. **Critical section** b. Entry section c. Remainder section d. All of these

80. Which memory is assembled between main memory and CPU:

    a. Primary memory b. **Cache memory** c. Both a & b d. None of these